A GaAs Double-Balanced Dual-Gate FET Mixer IC for UHF Receiver Front-End Applications

KUNIHIKO KANAZAWA, MASARU KAZUMURA, SHUTARO NAMBU, GOTA KANO, AND IWAO TERAMOTO

Abstract—**A double-balanced dual-gate FET mixer has been developed for application in the front-end circuit of UHF receivers.**

A 6–8-dB conversion gain has been obtained without an additional matching circuit over a wide frequency range from 100–800 MHz with good suppression of RF/LO feedthrough by more than 20 dB and third-order intermodulation product of −60 dB.

I. Introduction

IMPLEMENTATION OF the front-end circuit of a TV tuner is an attractive goal in applying GaAs analog IC's to consumer equipment [1]. Much effort has been devoted to achieving this goal, dealing mainly with low-noise wide-band amplifier circuits and mixer circuits.

Although wide-band amplifier circuits have made considerable progress recently [2]–[3], little achievement has been obtained for the mixer circuits [1], [4].

Essential problems to be discussed with respect to the monolithic mixer circuits are the gain, the intermodulation, the feedthrough of the RF/LO signals, and the matching circuits.

In this paper, we show that a new circuit configuration composed of the double-balanced dual-gate FET's can improve remarkably the RF performance of the mixer circuits. It is also demonstrated that the monolithic GaAs double-balanced dual-gate FET mixer IC has been successfully fabricated exhibiting a 6–8-dB conversion gain over a wide frequency range from 100–800 MHz with extremely suppressed feedthrough and intermodulation products without additional matching circuits. In the following, the design and fabrication of the monolithic GaAs double-balanced dual-gate FET mixer IC are described in full detail.

II. Modeling of the Dual-Gate FET Mixer

Prior to designing the double-balanced FET mixer IC, the principle of mixing operation of the dual-gate FET is discussed.

A small-signal equivalent circuit of the dual-gate FET is shown in Fig. 1, where the dual-gate FET is regarded as two single-gate FET's (FET1, FET2) connected in series [5]. RF and LO signals are applied to the first and second gates respectively so that the mixed IF signal can be extracted from the drain. It is useful to introduce ideal filters F_i $(i=0,1,2,3)$, which possess zero impedances at desired frequencies, at the input and output ports so as to separate the desired frequency from all after frequencies [4].

Essential parameters required for designing the practical mixer IC are the conversion gain and the third-order intermodulation product. We now assume that in the dual-gate FET mixer frequency mixing occurs only in FET2 while FET1 operates as an RF signal amplifier under a condition that the first gate is biased near the pinchoff voltage. For simplicity of the analysis, we also assume that only the transconductance has a time-varying function while the other parameters are constants.

The conversion gain G_c which is identical to the ratio of the IF output power to the RF source power is given by [4]

$$G_c = \frac{|I_{\mathrm{if}}|^2 \cdot \mathrm{Re}\, Z_L}{|E_{\mathrm{rf}}|^2/4 \cdot \mathrm{Re}\, Z_S} \tag{1}$$

where

I_{if} IF current,
E_{rf} RF source voltage,
Z_L load impedance,
Z_S source impedance.

The amount of suppression of the third-order intermodulation product IM_3 is defined as

$$\mathrm{IM}_3 = \frac{|I_{\mathrm{if}}|^2 \cdot \mathrm{Re}\, Z_L}{|I_{\mathrm{im3}}|^2 \cdot \mathrm{Re}\, Z_{L\,\mathrm{im3}}} \tag{2}$$

where

I_{im3} current of the third-order intermodulation product,
$Z_{L\,\mathrm{im3}}$ load impedance for I_{im3}.

The present task is to calculate I_{if} for G_c and I_{im3} for IM_3 using the equivalent circuit of Fig. 1.

The Taylor expansion of the transconductance g_{m1} of FET1 for the small RF signal $\Delta V_{g1}(t)$ becomes

$$g_{m1}(t) = g_{m10} + g_{m11} \cdot \Delta V_{g1}(t) + g_{m12} \cdot \left[\Delta V_{g1}(t)\right]^2 + \cdots. \tag{3}$$

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The authors are with the Semiconductor Laboratory, Matsushita Electronics Corporation, Takatsuki, Osaka 569, Japan.

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g_{m10} is a fundamental transconductance while the other g_t are the origins of the intermodulation distortion.

The RF output voltage V_{out1} of FET1 is given by

$$V_{out1} = \frac{g_{m10}}{G_{d1}} \cdot V_{g1} \tag{4}$$

$$= Z_b \cdot \frac{E_{rf}}{Z_a} \tag{5}$$

where

$$Z_a = Z_1 + R_{in1} + \frac{1}{j\omega_1 C_{gs1}}$$

$$R_{in1} = R_{s1} + R_{i1} + R_{g1}$$

$$Z_b = \frac{g_{m10}}{j\omega_1 \cdot C_{gs1} \cdot G_{d1}}$$

and where ω_1 is the RF frequency.

Mixing occurs in FET2 where the small-signal parameters are modulated at a periodic rate by a large LO signal applied to the second gate. The Fourier series of the transconductance g_{m2} of FET2 can be expressed as

$$g_{m2}(t) = \sum_{K=-\infty}^{\infty} g_{m2K} \cdot e^{jK\omega_0 t} \tag{6}$$

where

$$g_{m2K} = \frac{1}{2\pi} \int_0^{2\pi} g_{m2}(t) \cdot e^{-jK\omega_0 t} d(\omega_0 t) \tag{7}$$

ω_0 is the local frequency.

Since the frequency conversion from RF to IF occurs owing to the existence of g_{m21}, the IF output voltage V_{out2} from FET2 becomes

$$V_{out2} = V_{g2} \cdot \frac{g_{m21}}{G_{d2}}$$

$$= \frac{Z_b \cdot Z_d \cdot E_{rf}}{Z_a \cdot Z_c} \tag{8}$$

where

$$V_{g2} = \frac{V_{out1}}{Z_c} \cdot \frac{1}{j\omega_1 C_{gs2}}$$

$$Z_c = R_{s1} + R_{d1} + R_{in2} + Z_3 + \frac{1}{G_{d1}} + \frac{1}{j\omega_1 C_{gs2}} + \frac{\left(R_{s1} + R_{d1} + R_{s2} + \frac{1}{G_{d1}}\right) \cdot \left(R_{i2} + R_{g2} + Z_3 + \frac{1 + g_{m20}/G_{d2}}{j\omega_1 C_{gs2}}\right)}{R_{d2} + Z_7 + 1/G_{d2}}$$

$$R_{in2} = R_{s2} + R_{i2} + R_{g2}$$

$$Z_d = \frac{g_{m21}}{j\omega_1 C_{gs2} \cdot G_{d2}}.$$

The IF current I_{if} at the drain port in Fig. 1 is given by

$$I_{if} = \frac{V_{out_2}}{Z_e} \tag{9}$$

where

$$Z_e = Z_8 + R_{d2} + \frac{1}{G_{d2}} + \frac{A \cdot B}{A + B}$$

$$A = R_{s1} + R_{d1} + R_{s2} + \frac{1}{G_{d1}}$$

$$B = R_{i2} + R_{g2} + Z_4 + \frac{1}{j\omega_2 C_{gs2}}$$

and where ω_2 is the IF frequency.

Using (1), (8), and (9), the conversion gain G_c is obtained as

$$G_c = 4 \cdot R_{G1} \cdot R_L \cdot \left| \frac{Z_b \cdot Z_d}{Z_a \cdot Z_c \cdot Z_e} \right|^2 \tag{10}$$

where

$$Z_S = Z_1$$

$$= R_{G1} + jX_{G1}$$

$$Z_L = Z_8$$

$$= R_L + jX_L.$$

The next item to be discussed is the intermodulation in the dual gate FET which is caused by the interference signal of a frequency ω_1' near ω_1. Among the various frequency components, the third-order intermodulation products $|\omega_0 \pm (2\omega_1 - \omega_1')|$ and $|\omega_0 \pm (2\omega_1' - \omega_1)|$ are important because they are very close to the IF frequency ω_2. These third-order intermodulation products result from mixing between the first term of the LO signal and the second term of g_{m1} for FET1.

If an interference signal level is equal to that of the RF signal, the output voltage of the third-order intermodulation in FET2 can be derived in the same way as used for the G_c calculation. Thus, we have

$$V_{im3} \simeq \frac{Z_b' \cdot Z_d \cdot (E_{rf})^3}{(Z_a)^3 \cdot Z_c} \tag{11}$$

where

$$Z_b' = \frac{g_{m12}}{(j\omega_1 C_{gs1})^3 \cdot G_{d1}}.$$

In (11), $\omega_4 (= |2\omega_1' - \omega_1| \text{ or } |2\omega_1 - \omega_1'|) \simeq \omega_1$ is assumed so that $Z_{L\,im3} \simeq Z_L$ can be used. The current of the third-order intermodulation product I_{im3} at the drain port in Fig. 1 is

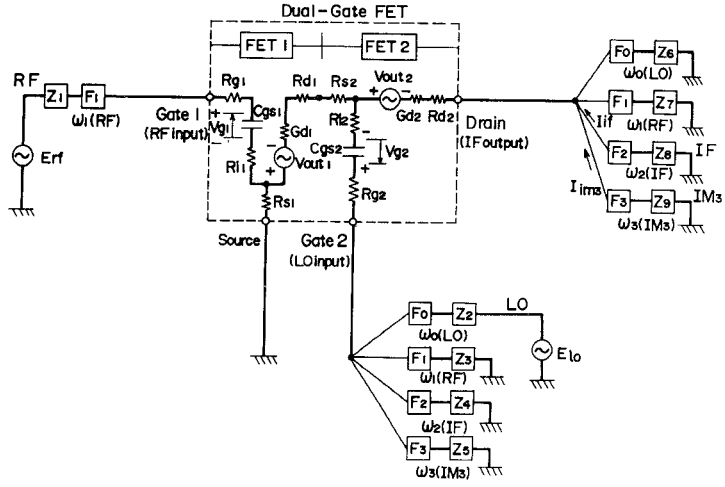

Fig. 1. Schematic of FET mixer, including signal, third-order intermodulation, and IF circuits, used in signal analysis.

given by

$$I_{im3} = \frac{V_{im3}}{Z_e}. \tag{12}$$

Using (2), (8), (9), (11), and (12), the amount of suppression of the third-order intermodulation product IM_3 is obtained as

$$IM_3 = \left\{ \frac{g_{m10}}{g_{m12}} \cdot (\omega_1 C_{gs1})^2 \right\}^2 \cdot \frac{\left\{ (R_{G1} + R_{in1})^2 + \left(X_{G1} - \frac{1}{\omega_1 C_{gs1}} \right)^2 \right\}^2}{|E_{rf}|^4}. \tag{13}$$

III. Design and Fabrication of the Double-Balanced Dual-Gate FET Mixer IC

A goal of the present work is to design and fabricate a double-balanced dual-gate FET mixer IC for use in the receiver front-end that covers the VHF to UHF bands. The circuit to be designed is shown in Fig. 2. Note that the circuit consists of four dual-gate FET's.

The RF and LO signals are applied through the baluns, as this figure indicates. The double-balanced mixer circuit is featured because of good suppression of the RF and LO feedthrough and the even-order intermodulation products.

A. Design

A target specification of the present development is summarized in Table I.

The conversion gain G_c of the dual-gate FET of (10) was calculated as a function of the gate width Wg assuming the FET parameters as listed in Table II. Those parameters are obtainable practically for the single-gate GaAs MESFET with a 1-μm gate length. In Fig. 3 are shown calculated results of the conversion gain as a function of the gate width Wg for the different source/load impedances Z_S ($= Z_1$) and Z_L ($= Z_8$). Although it is desirable for the source/load impedances to be 50 Ω for practical applications, the result of Fig. 3 indicates that use of 50 Ω requires a large gate width Wg in order to satisfy the target conversion gain of 5 dB resulting in increased power consumption and chip size. Therefore, we designed the source/load impedances to be $Z_S = Z_L = 200$ Ω, and therefore use of the 1:4 balun is necessary. The calculated result of the

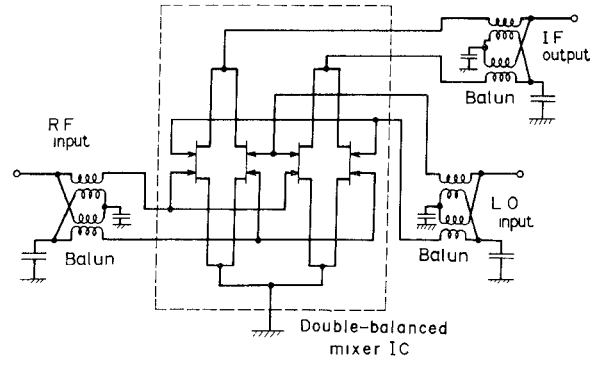

Fig. 2. Circuit diagram of the monolithic mixer IC.

TABLE I
Target Specification of the Present Development

RF Performance	Design Target	Condition
Conversion Gain	>5 dB	f_{RF} = 100-1000MHz P_{LO} = 10 dBm
Suppression Ratio of the Third-order Intermodulation Product	>60 dB	P_{RF} = -20 dBm P_{LO} = 10 dBm

TABLE II
FET PARAMETERS (Wg[μm])

R_S	$1.5 \times 10^3 / Wg$ (Ω)
R_i	$9.0 \times 10^2 / Wg$ (Ω)
R_g	$1.7 \times 10^{-2} \times Wg$ (Ω)
C_{gs}	$1.3 \times 10^{-3} \times Wg$ (pF)
R_d	$2.1 \times 10^3 / Wg$ (Ω)
G_d	$6.7 \times 10^{-6} \times Wg$ (S)
g_{m10}	$8.0 \times 10^{-5} \times Wg$ (S)
g_{m12}	$2.0 \times 10^{-5} \times Wg$ (S)
g_{m21}	$4.3 \times 10^{-5} \times Wg$ (S)
(P_{LO} = 10dBm)	

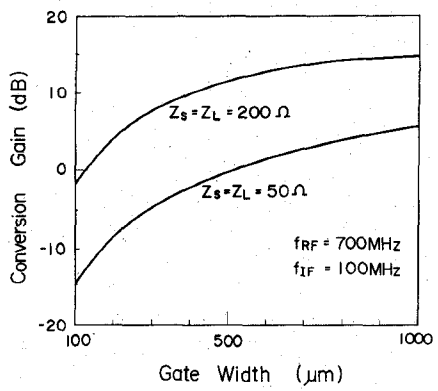

Fig. 3. Calculated conversion gain as a function of the gate width.

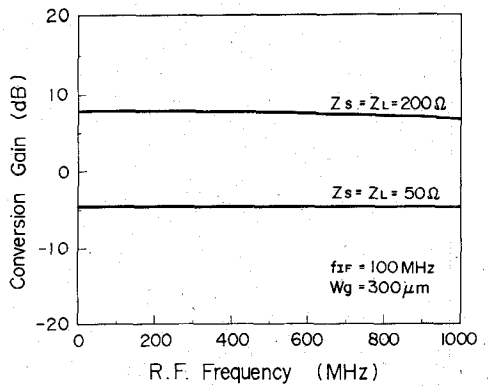

Fig. 4. Calculated conversion gain as a function of the RF frequency.

conversion gain for $Z_S = Z_L = 200\ \Omega$ indicates that the target of 5-dB conversion gain can be obtained by taking $Wg = 300\ \mu$m.

The RF frequency dependence of the conversion gain G_c was calculated for the dual-gate FET with a 300-μm gate width. The IF frequency is assumed to be 100 MHz. The calculated results are shown in Fig. 4, where it is noted that the conversion gain maintains an almost constant value over a wide frequency range from 0–1000 MHz. It is also to be noted that the double-balanced circuit with 200-Ω source/load impedances provides a gain by about 12 dB higher than that with 50-Ω source/load impedances.

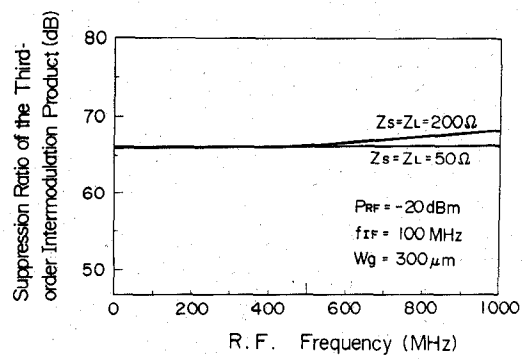

Fig. 5. Calculated suppression ratio of the third-order intermodulation product as a function of the drain current.

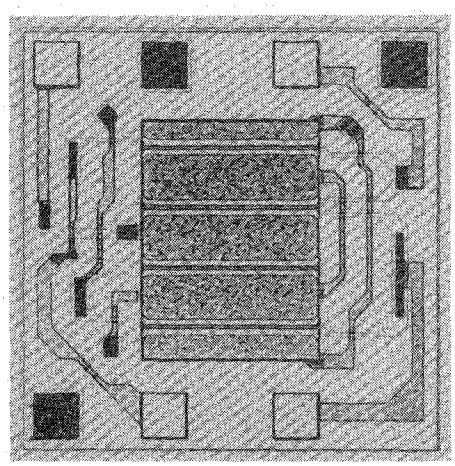

Fig. 6. Photograph of the completed mixer IC.

Fig. 5 shows the calculated results of the third-order intermodulation products given by (13) for the FET with a 300-μm gate width. The interference signal level is assumed to be -20 dBm, which is identical to that of the RF signal. It is seen that the third-order intermodulation product is suppressed down to about -66 dB over a wide frequency range from 0–1000 MHz, which satisfies the target specification of the present work.

B. Fabrication and RF Performance

The GaAs double-balanced dual-gate FET mixer IC was fabricated. The n-type active and n^+-type contact layers were provided by selective ion implantation of Si onto a nondoped semi-insulating GaAs substrate under a condition of 5×10^{12} cm^{-2} (dose) at 130 keV and 5×10^{13} cm^{-2} (dose) at 150 keV, respectively. The multimetal layers of Au/Ni/AuGe and Al/Ti were used as ohmic and gate electrodes, respectively. The interconnection was provided by a Au/Ti double layer.

A photograph of the experimental chip is shown in Fig. 6.

A measurement set up to determine the conversion gain and the third-order intermodulation product is shown in Fig. 7. Measurements were carried out without input and

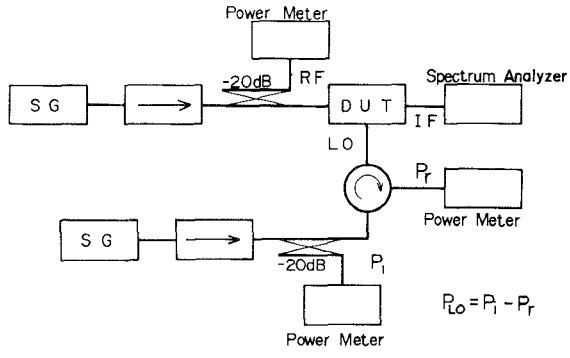

Fig. 7. Measurement setup for the gain and the third-order intermodulation product.

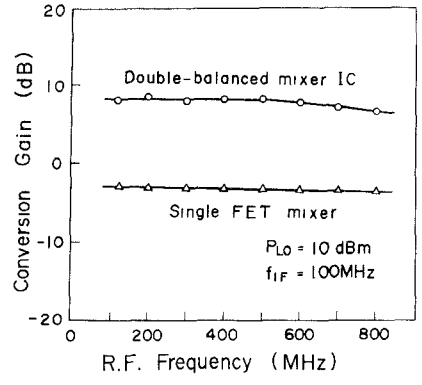

Fig 8. Conversion gain of the experimental IC as a function of the RF frequency comparing with that of the single FET mixer.

output matching circuits. The LO power level was calibrated by subtracting the reflective power.

Fig. 8 shows the conversion gain measured as a function of RF frequency, where the IF frequency was 100 MHz. The signal power levels of RF and LO inputs were -20 dBm and 10 dBm, respectively. The ferrite core baluns were used for each I/O port. The loss ($0.5 \sim 1.0$ dB at 100–800 MHz) which originates in the balun was subtracted from the measured conversion gain. It is to be noted that the experimental mixer IC exhibits a very high conversion gain of 6–8 dB over a wide frequency range from 100 to 800 MHz. Decrease in the conversion gain at higher frequency is due to the loss caused by parasitic capacitances. The measured conversion gain of the single FET mixer with the same geometry is also shown in Fig. 8 for comparison. It is noteworthy that the conversion gain of the present double-balanced mixer exceeds that of the single mixer with 50-Ω source/load impedances by about 12 dB. It is also noted that the experimental data show fairly good agreement with the calculated results shown in Fig. 4.

Fig. 9 shows the suppression ratio IM_3 of the measured third-order intermodulation product and the conversion gain as a function of the drain current I_D. The RF signal at 700 MHz and the interference signal at 701 MHz were both -20 dBm and the LO signal was $+10$ dBm. The measured third-order intermodulation product arises at 101 MHz. The value of the suppression ratio IM_3 of the

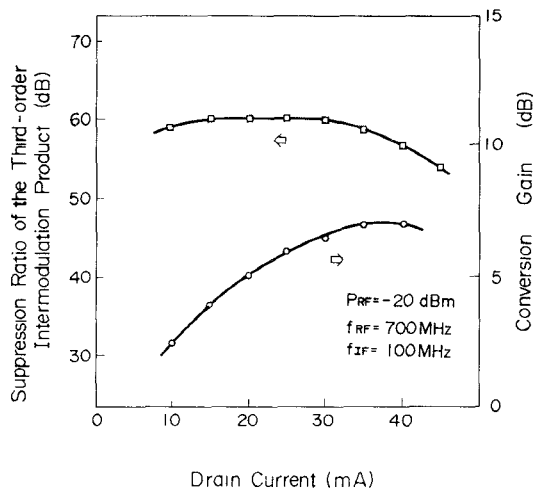

Fig. 9. Suppression ratio of the third-order intermodulation product and conversion gain as a function of the drain current.

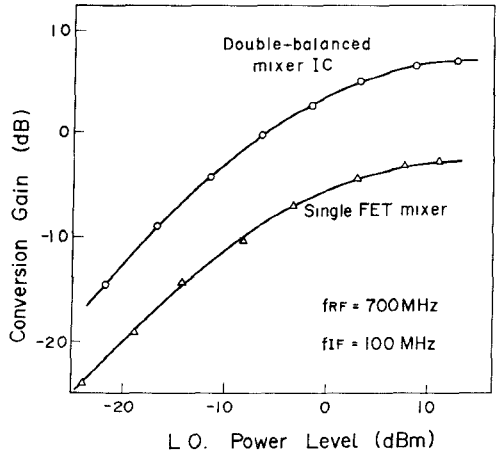

Fig. 10. Conversion gain of the experimental IC as a function of the LO power.

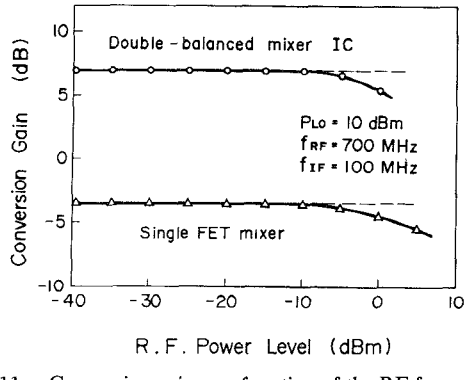

Fig. 11. Conversion gain as a function of the RF frequency.

obtained third-order intermodulation product was smaller than that expected from the theory. This is due to the fact that the nonlineality of the drain conductance G_d and the drain-source capacitance C_{gs} are neglected in the theoretical equation.

The measured conversion gain are shown in Figs. 10 and 11 as functions of the LO power and the RF power,

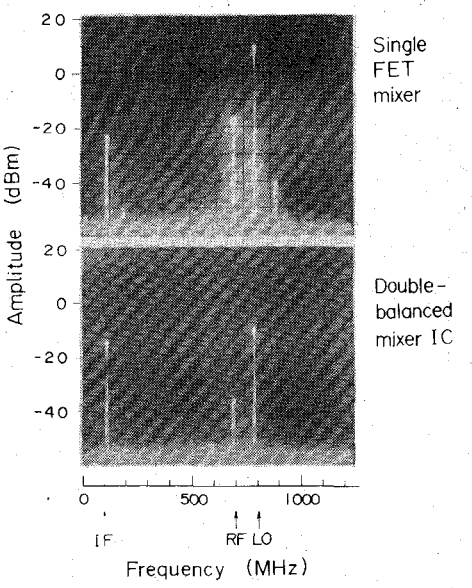

Fig. 12. Output frequency spectrum of the experimental IC compared with that of the single FET mixer: $P_{LO} = 10$ dBm, $P_{RF} = -20$ dBm.

respectively. The 1-dB compression point of gain of the experimental mixer IC is at about −2-dBm RF power level.

In Fig. 12 are shown the output frequency spectra for the single FET mixer and the double-balanced FET mixer IC. The RF power level is −20 dBm and the LO power level is 10 dBm. It is seen that the double-balanced mixer IC exhibits excellent suppression of the LO and RF feedthrough as well as the higher order mixing products comparing the single FET mixer. The suppression is more than 20 dB.

IV. Conclusion

A model of the dual-gate FET mixer was presented. The conversion gain and the intermodulation products were analytically discussed. The double-balanced dual-gate FET mixer IC has been designed and fabricated on the basis of the present model. High conversion gain of 6–8 dB was obtained over a wide frequency range from 100 to 800 MHz without additional matching circuits. The RF and LO feedthrough and the higher order distortion were well suppressed by more than 20 dB.

This GaAs double-balanced dual-gate FET mixer IC would be a promising candidate for VHF/UHF receiver front-end applications.

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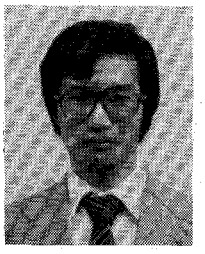

Kunihiko Kanazawa was born in Kyoto, Japan, on November 21, 1955. He received the B.S. and M.S. degrees in electronics engineering from Kyoto University, Kyoto, Japan, in 1979 and 1981, respectively.

He joined the Research Laboratory of Matsushita Electronics Corporation, Takatsuki, Osaka, Japan in 1981, where he has been engaged in the research and development of GaAs IC's.

Mr. Kanazawa is a member of the Institute of Electronics and Communication Engineers in Japan and the Japan Society of Applied Physics.

Masaru Kazumura received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1970 and 1972, respectively.

He joined the Matsushita Electronics Corporation, Osaka, Japan, in 1972, where he has been engaged in the research and development of compound semiconductor devices. He is currently Manager of the Microwave Device Group, Semiconductor Laboratory of Matsushita Electronics Corporation.

Shutaro Nambu was born in Ishikawa Prefecture, Japan, on February 24, 1946. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1968, 1970, and 1978, respectively.

In 1970, he joined the Matsushita Electronics Corporation, Takatsuki, Osaka, Japan. From 1971 to 1976, he worked on the microwave integrated circuit solid-state oscillator and other MIC components. Since 1978, he has been engaged in the research and development of GaAs FET's and integrated circuits. He is currently manager of the High Frequency Device Division at the Semiconductor Group of the Matsushita Electronics Corporation.

Dr. Nambu is a member of the Institute of Electronics and Communication Engineers of Japan.

Gota Kano was born in Osaka, Japan, in October 2, 1938. He received the B.S. degree in 1961 and the Ph.D. degree in 1970, both in electrical engineering, from Osaka University, Osaka, Japan.

He first joined the Research Laboratory of the Matsushita Electronics Corporation, Takatsuki, Osaka, Japan, where he was engaged in the research and development of semiconductor devices, such as tunnel diodes, Schottky diodes, and high-speed bipolar integrated circuits. His most recent activities have included the development of GaAs FET's, GaAs IC's, and semiconductor lasers.

He presently heads the Advanced Device Development Department of the Semiconductor Laboratory of the Matsushita Electronics Corporation.

Iwao Teramoto was born in Osaka, Japan, on January 29, 1932. He received the B.S., M.S., and Ph.D. degrees in engineering chemistry from Kyoto University, Kyoto, Japan, in 1954, 1956, and 1964, respectively.

Joining the Matsushita Electronics Corporation, Takatsuki, Osaka, Japan, in 1956, he worked in research on solid-state chemistry. From 1964 to 1965, he was a Research Chemist with the Philips Research Laboratories, Eindhoven, The Netherlands. He is presently the Director of the Semiconductor Laboratory of the Matsushita Electronics Corporation.

Dr. Teramoto is a member of the Physical Society of Japan, the Institute of Electronics and Communication Engineers of Japan, and the Electrochemical Society of America.